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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/938,496	08/27/2001	Hideo Miyake	1614.1181	2883

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EXAMINER	
BATES, KEVIN T	
ART UNIT	PAPER NUMBER
2153	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/938,496	MIYAKE ET AL.	
	Examiner	Art Unit	
	Kevin Bates	2153	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-5,7,8,10-13,15-18 and 20-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-5, 7-8, 10-13, 15-18, and 20-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

This Office Action is in response to a communication received on November 13, 2007.

Claims 1, 6, 9, 14, and 19 have been cancelled.

Claims 23 has been added.

Claims 17, 21, and 22 have been amended.

Claims 2-5, 7-8, 10-13, 15-18, and 20-23 are currently pending in this application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 5, 8, 10, 13, 16, 16-18, and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Computer Organization & Design (Computer Organization & Design; Patterson et. al.) (Hereinafter Patterson) in view of Tanaka (5815696).

Regarding claims 17, 21, and 22, Patterson teaches a computer which processes an interrupt of a program caused by an exception operation when an instruction is executed (Page 223, Paragraph 1), said computer comprising:

A data holding part holding said instruction when the instruction processing starts (Page 223, Paragraph 1), wherein the computer processing method performs interput processing by an interrupt processing program by reading the address of the instruction from the memory to return from the interrupt (Page 223, Paragraph 1).

Patterson does not explicitly indicate that there are a plural instructions in parallel and having the memory store the addresses of the plural instructions during the interrupt and that the program uses the plurality of addresses to return for the interrupt.

Tanaka teaches an interrupt system that includes storing the addresses of instructions operating in parallel when an interrupt occurs (Column 3, line 65 – Column 4, line 4) and that the program uses the plurality of addresses to return for the interrupt (Column 4, lines 5 – 8).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Tanaka's teaching in order to allow Patterson's system to operating an a parallel or pipelined instruction system and to recover interrupts quickly and effectively.

Regarding claim 23, Patterson teaches a method comprising: storing in a data holding unit an instruction being executed in processing and interrupt processing an instruction at a time when an interrupt starts (Page 223, Paragraph 1); and performing interrupt processing using the interrupt processing instruction stored in the data holding unit to return from the interrupt (Page 223, Paragraph 1).

Patterson does not explicitly indicate that there are a plural instructions in parallel and having the memory store the addresses of the plural instructions during the interrupt and that the program uses the plurality of addresses to return for the interrupt.

Tanaka teaches an interrupt system that includes storing the addresses of instructions operating in parallel when an interrupt occurs (Column 3, line 65 – Column 4, line 4) and that the program uses the plurality of addresses to return for the interrupt (Column 4, lines 5 – 8).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Tanaka's teaching in order to allow Patterson's system to operating an a parallel or pipelined instruction system and to recover interrupts quickly and effectively.

Regarding claims 2 and 10, Patterson teaches that the storage medium is a plurality of registers (Page 223, Paragraph 1).

Regarding claims 5 and 13, Patterson teaches that said data holding part holds an instruction address of an instruction which causes said interrupt (Page 223, Paragraph 2).

Regarding claims 8, 16, and 18, Patterson teaches that said data is used for recovery from said interrupt (Page 223, Paragraph 2).

Regarding claim 20, Patterson teaches that the interrupt processing is initiated by an exception operation (Page 223, Paragraph 1).

Claims 3-4, 7, 11-12, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Computer Organization & Design; Patterson et. al. in view of Sakamura, and in further view of Cheong (6098167).

Regarding claims 4 and 12, Patterson teaches the computer claimed in claims 21 and 22.

Patterson does not explicitly indicate that when a stored instruction gets interrupted, said store instruction requested said data is stored at the data storing part.

Cheong teaches a system for allowing interrupts of instructions, where there is a data holding part for holding the interrupted instruction (Column 15, line 64 – Column 16, line 3), that data from the instruction is maintained (Column 15, line 64 – Column 16, line 3) and that this includes store instructions (Column 16, lines 5 – 7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Cheong's teaching of holding more information about the interrupted instruction in Patterson in order to allow out of order processing while maintaining storage consistency.

Regarding claims 7 and 15, Patterson teaches the computer in claims 21 and 22.

Patterson does not explicitly indicate wherin said data holding part holds an effective address of a load or store instruction when said interrupt occurs during said instruction.

Cheong teaches a system for allowing interrupts of instructions, where there is a data holding part for holding the interrupted instruction (Column 15, line 64 – Column

16, line 3), that data from the instruction is maintained (Column 15, line 64 – Column 16, line 3) and that this includes store and load instructions (Column 16, lines 5 – 7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Cheong's teaching of holding more information about the interrupted instruction in Patterson in order to allow out of order processing while maintaining storage consistency.

Regarding claims 3 and 11, Patterson teaches the computer in claims 2 and 10.

Patterson does not explicitly indicate teaches that flags indicate whether said data is held in said register.

Cheong teaches that flags indicate whether said data is held in said register (Column 16, lines 43 – 51).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Cheong's teaching of holding more information about the interrupted instruction in Patterson in order to allow out of order processing while maintaining storage consistency.

Response to Arguments

Applicant's arguments with respect to claims 17, 21, and 22 have been considered but are moot in view of the new ground(s) of rejection.

Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No. 5561774 issued to Aikawa because it teaches using traps and interrupts in a parallel processing system.

U. S. Patent No. 4541047 issued to Wada, because it teaches recovering from interrupts in a pipelined processor.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Bates whose telephone number is (571) 272-3980. The examiner can normally be reached on 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glen Burgess can be reached on (571) 272-3949. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kevin Bates
December 17, 2007

GLENTON B. BURGESS
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